

# Router Design for Optical Cartesian Networks

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## Abstract

*The paper describes the progress in the research, design, and development of an all-optical router for the optical switching of packets in Cartesian Networks (a novel network akin to mesh networks). The importance of all-optical packet switching/routing for convergent, next generation transport network is described. The selection of Cartesian routing as the basic routing methodology for all-optical packets is justified. The photonic packet switch/router architecture is studied in detail. Various design issues related to an all-optical node, such as header synchronization, header processing and optical buffering have been addressed. The functionality modelling of optical components and optical switch/router simulation algorithms are presented as well.*

## 1. Introduction

The ever increasing growth in Internet traffic is driving the demands for higher transmission capacity and higher processing speed. The processing capacity of electronic routers is rapidly approaching the electronic bottleneck, and yet the need for high throughput in backbone networks is still not satisfied. One possible solution to this limitation is to change packet processing from electronic to optical: Wavelength Division Multiplexing (WDM) technology provides a platform to exploit the potential bandwidth of optical fibers to solve the capacity problem.

However, the lack of integrated optical circuits capable of performing IP address resolution has resulted in hybrid optical nodes where transmission and switching are performed in the optical domain, while routing and forwarding are done electronically [1].

Although WDM increases the bandwidth of the fiber enormously depending upon the number of wavelengths per fiber [2], it also places a tremendous burden on the electronic switches and routers at each node that must perform all this processing [3]. The situation results in an electronic bottleneck, whereby the transmission capacity of the optical network is being throttled by the electronics, as the

theoretical limit of the digital processing speed (10 Gbps) is far less than that of the optical domain [3].

One of the major reasons for the limited throughput capabilities of the electronic router is that the existing hierarchical routing schemes employ distance vector and link state routing algorithms, which require the exchange of routing information for the construction and maintenance of routing tables [4]. As networks increase in size, the memory requirements for the routing tables and the time taken to search the tables increase proportionally [4]. Optical implementation of a router based on these routing schemes would require querying an optical lookup table which, at present, is not feasible given the current under-developed state of optical buffering.

This paper discusses the design and implementation of an optical router that is to be deployed in a novel packet routing technology known as Cartesian routing, which overcomes many of the problems associated with hierarchical routing schemes. There are no routing tables and limited state information is exchanged between routers: the route calculation is neither memory nor CPU intensive [4].

The organization of the remainder of the paper is as follows: Section 2 gives a brief introduction to Cartesian Networks. To implement all-optical routing, the actualization of the network depends on the development of compact and low cost optical devices, therefore section 3 presents a brief analysis on one of the most important devices used in WDM systems: SOA-MZI. The working principle of the device, along with one of its application is discussed. Section 4 demonstrates how these devices can be incorporated for designing an all-optical router to route packets optically in Cartesian Networks. Simulation result verifying the functionality of the design in section 5. Section 6 concludes this paper examining different areas that need to be addressed to make the proposed design for the all-optical router to be fully operational in Cartesian Networks.

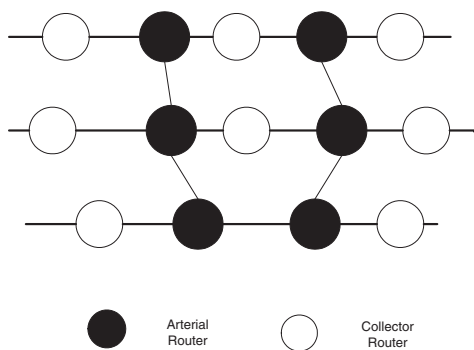
## 2. Cartesian Networks

When a packet arrives at a conventional router, the router uses a routing table to determine whether to keep, forward,

or discard the packet and if forwarding the packet, on which link the packet should be forwarded [5].

The Cartesian unicast routing methodology, which is based upon two distinct co-operative linear routing algorithms, differs from existing provider-based unicast routing in that routers maintain a minimal amount of state information. Routing tables are unnecessary since communications are topologically dependent, thus potentially reducing router and network overheads [4]. By comparing the packet's destination address with its own address (both expressed in latitude and longitude), the router knows whether to keep, forward in the direction of dispatch, or discard the packet, without the use of a routing table [4]. This eliminates the need to maintain and search a database of network state information, thereby reducing the time taken for the routing decision from  $O(\log(n))$  to  $O(n)$  in the conventional networks, to  $O(1)$  in Cartesian routing [4].

As shown in figure 1, the Cartesian topology is composed of two or more horizontal 'subnetworks', or collectors, consisting of routers connected horizontally and sharing a common horizontal identifier such as latitude. Collectors are interconnected by one or more vertical subnetworks, or arterials, consisting of routers connected vertically. Arterials need not share a common vertical identifier. The address structure indicates the location of a router in two dimensions; that is, the router's location is specified in terms of its horizontal and vertical positions, such as latitude and longitude. Collector routers have two ports (east and west) to exchange packets "horizontally", while the arterials exchange packets between collectors [4].



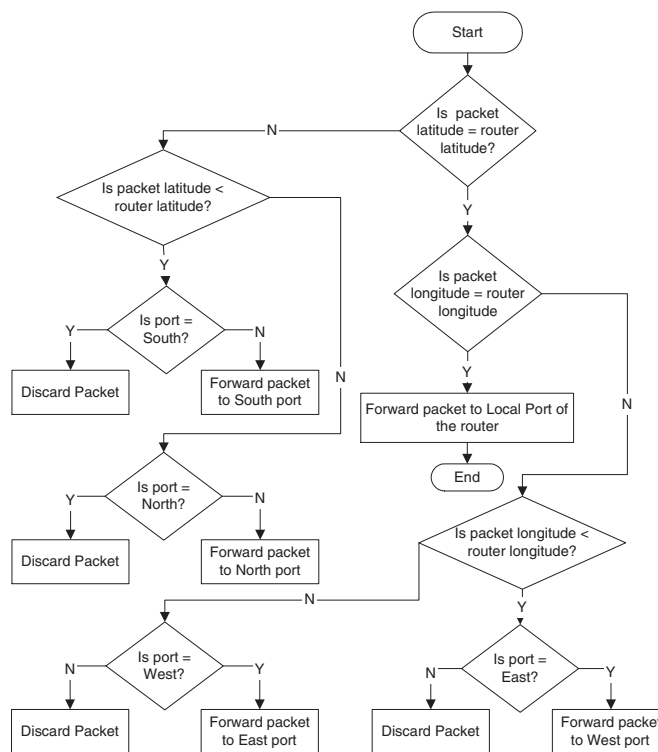
**Figure 1. Cartesian Network**

As the paper discusses a proposed solution for the Arterial Router, its routing algorithm is described below.

### 2.1. Arterial Router

If a packet's destination address is on a different collector, the source collector sends the packet to an arterial router so as to send the packet in the direction of the destination collector. The routing algorithm is slightly more complex

for the arterial router (see figure 2) than that of the collector router, as packets can arrive from four possible directions (East, West, North or South) as opposed to collector router which performs only east-west routing.



**Figure 2. Process flow for Arterial Router**

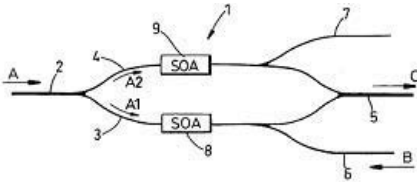
To prevent packet oscillation, a packet is forwarded in any other direction except that on which it arrived [4]. If the destination latitude is not equal to that of the arterial, then the packet is forwarded north or south, otherwise it is forwarded east or west.

In order to make such a network operational in the optical domain, all-optical devices have to be utilized to build the corresponding routers. One such device, the SOA-MZI; is described in Section 3.

### 3. SOA-MZI - The Basic Building Block

The basic optical device 'building block' is the Semiconductor Optical Amplifier-Mach Zehnder Interferometer (SOA-MZI) [6].

The simplest SOA-MZI setup is shown in figure 3. Both the SOAs (8) and (9), are supplied with bias currents that are maintained at controlled levels and are determined according to a required phase relationship between the optical signals transmitted to the output waveguide (5) [7]. The input signal A, upon entering the waveguide (2), is split through a "Y" splitter into two components A1 and



**Figure 3. SOA-MZI setup [6]**

A2. A second input signal B is injected from arm (6) and is counter propagated through arm (3), thus modulating the phase of the first input signal in the lower arm through a process of cross phase modulation (XPM) [6].

When there is no phase delay, the signal is recombined at the “Y” junction (coupler) immediately before the light exits the SOA-MZI device through output waveguide (5) [8]. Since the signals in each arm are coherent with each other, they are reinforced during recombination and constructive interference takes place [6]. When there is a phase difference at the output of the Y-coupler, the signals will be out of phase with one other. When these signals recombine, some (or all) of the optical power will be lost because the signals interfere with each other. If the phase difference is  $\Pi$ , then output will be zero and destructive interference will take place [6].

Different biasing conditions are possible depending upon the absence of counter-propagating optical signals injected via the second and third input waveguides (6) and (7) of figure 3. These different biasing conditions lead to the manifestations of different optical logic [6]. The operation of the SOA-MZI device as an AND gate [6, 9] has been described below to illustrate the concept.

### 3.1. The optical AND gate

As shown in figure 3, if the second input signal B injected via waveguide (6) is low, then the semiconductor optical amplifiers (8) and (9), are biased such that, the first component, A1, experiences a phase shift of  $\Pi$  due to the non-linear properties of the amplifier material, resulting in cross-phase modulation when propagated through the first semiconductor optical amplifier. The resulting output signal C available at output waveguide (5), would then be modulated to a zero state by destructive interference between the out of phase first and second components, A1 and A2 (this bias condition is represented by  $\Delta\phi = \Pi$ ). In the presence of the counter-propagating second optical signal B, the phase of the first component, A1, is modulated by a phase increment of  $\Pi$ , such that the first and second components, A1 and A2, when being transmitted through the first and second arms (3) and (4), recombine with constructive interference at the output waveguide (5), thereby providing a logic state “1” as the output signal C. As a re-

sult, the biasing condition  $\Delta\phi = \Pi$ , gives a logic device performing the function “A AND B”.

A mathematical model of the SOA-MZI device, described in [10], has been used to model the device to operate as logical optical gates and the transfer function characteristics have been successfully simulated using MATLAB 6.5 [11]. Due to space constraints, the transfer characteristics along with the simulation results of the SOA-MZI device working as an optical gate has not been included in this paper.

## 4. Optical Routing in Cartesian Networks

An ideal optical packet switch should preserve end-to-end optical transparency (in terms of data rate, wavelength, and format) throughout the routing process [12]. This transparency allows the transmitted signal to stay in the optical form without undergoing electronic conversion during its path from the source to the destination [12]. A practical optical packet switch should route packets from switch input to output using simple routing procedures which are able to handle switch-level routing and contention resolution [12]. This section presents a practical design of an all-optical router for routing fixed length unicast packets optically in a Cartesian Network.

A critical assumption to note is that time is divided into equal timeslots, each containing one packet. For optical packet switching, fixed-length packets can simplify the design and operation of the network (and its switching nodes), and allowing for the transport of larger entities (e.g., IP datagrams) by fragmenting them into smaller, equal-sized packets.

A generic optical packet-switched node structure consists of three sub-blocks [1]:

- An input interface consisting of an (optical) synchronizer which aligns incoming packets in real time against a clock.
- A switching core that routes packets to their proper outputs and executes contention resolution using appropriate buffering schemes.
- An output interface which inserts a new header and may have to regenerate the data.

Though the paper touches on the above topics briefly, the authors primarily focus on the routing aspect of the optical node. A step-by-step analysis is presented describing the path of an optical packet from the point when it arrives at an arterial router, until it is routed to the appropriate output port.

## 4.1. Packet Synchronization

It is assumed that packets entering the switch are aligned with their respective timeslots. Such synchronization is generally a requirement for correct switching operation. Approaches to achieving packet synchronism at the inputs to the switches constitute a topic in its own right [1] and are beyond the scope of this paper.

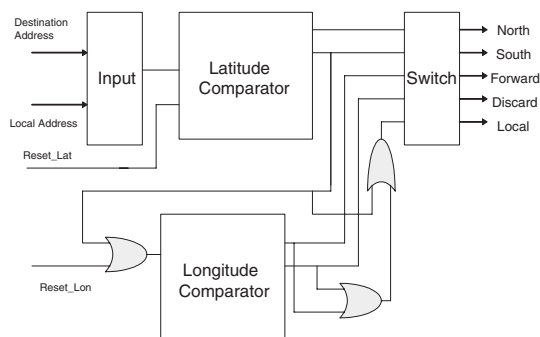
## 4.2. Routing/Switching

With an aim to incorporate the Arterial router algorithm for optical routing in Cartesian Networks, an all-optical arterial router which performs the header processing, and the routing of optical packets is now described.

All the gates shown in the circuit are optical gates based on the SOA-MZI device, as described in section 3. They are represented in the electronic gates convention to clarify the operations within the circuit.

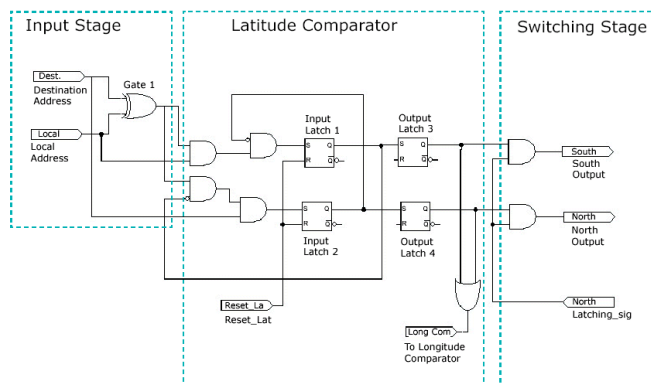
### 4.2.1 Router Design

The block diagram for the optical arterial router is shown below in figure 4.



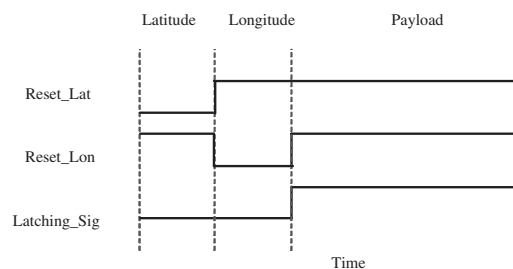
**Figure 4. Block diagram of all-optical Arterial router**

The entire circuit is divided into four sections. The first section comprises of the input stage, where the two addresses: the destination address of the incoming packet and the local address of the node are compared bit by bit, starting with the most significant bit first. The second section is the Latitude comparator, which checks whether the latitude of the incoming packet is the same as that of the node itself. The longitude comparator compares the longitude portion of the two packets. Finally the switching stage switches the packet to the appropriate port. The operation of the latitude comparator is described below. The schematic is shown in figure 5, which depicts the input and the latitude comparator stages and a part of the switching stage.



**Figure 5. Latitude Comparator**

The operation of the router is based on three control signals. These signals are shown below in figure 6. It is assumed that all of these signals and the arrival of the incoming and the local packet, are synchronized in the fixed length time for the packet switching operation. The Reset\_Lat signal remains low while the latitude part of the address is being compared and then goes high during longitude comparison, thus resetting the input latches 1 and 2 in the Latitude comparator block and making it inactive during the longitude comparison. During the latitude comparison, even though the longitude comparator would be receiving the incoming bits, there is no output is available at this block as the Reset\_Lon is set, disabling the input latches of the longitude comparator block. This is important as only a single output latch is set during the entire operation of address comparison, thus indicating the port to which the packet is routed.



**Figure 6. Control Signals for the operation of Arterial Router**

There are two cases related to latitude comparison: the incoming packet's destination latitude is same as the latitude of the local node, or both are different.

If the latitudes are same, then the output of the gate 1 (see figure 5) in the input stage would be low, which in turn

would cause the outputs of the corresponding gates in the latitude comparator stage to be low. As a result, none of the input latches 1 and 2 would be set and hence at the end of the latitude comparison the output of the latitude comparator block would be low, meaning that the packet is not to be sent either north or south, but it is to be sent to a router on the same latitude or to be discarded. Hence longitude comparison would take place to determine the exact position of the destination router.

The Reset\_Lat signal goes high at the end of the latitude address comparison and resets the input latches 1 and 2 of the Latitude comparator for the remainder of the longitude address comparison. At the same time, the Reset\_Lon goes low, enabling the input latches of the Longitude comparator, thus activating the longitude comparison operation.

During the longitude comparison, if an inequality is found between the longitudes, then the packet is either forwarded to the output port or discarded, depending upon whether the incoming packet's longitude is greater than that of the local packet's longitude or vice versa, respectively. If no inequality is detected, meaning that the packet is destined for the same node, then the local output would be enabled and the packet would be sent to the local port of the node. At the end of the entire address comparison, a Latching\_Sig (refer to fig 6) is set to high, so as to enable the port determined by the address comparison and the packet is forwarded to the respective port.

If the latitudes are different, then output of the gate 1 in figure 5 is high, which sets either of the input latches 1 or 2 depending upon whether the destination address of the incoming packet is less than that of the local address of the node or vice versa. This enables either of the output latches 3 or 4, and remains set for the rest of the address comparison. Once a latch is set during the latitude comparison, the input latches in the longitude comparator block are reset for the duration of the address comparison. This signifies that during the entire address comparison operation, once an inequality between the destination and the local address is detected, then regardless of the differences in the power level of the next incoming bits, a decision is made to determine the port to which the packet should be switched. Once the port is determined, the packet is sent to it after the end of the address comparison.

### 4.3. Related Issues

#### 4.3.1 Header Processing

This scheme approaches all-optical header processing in a unique manner, minimizing hardware costs and processing times. Unlike other optical node architectures, the header is not separated from the payload. Instead the entire packet, including the header and the payload, is subjected to the router for address comparison. As mentioned earlier, it is

assumed that both the incoming and the local packets are aligned with their time slot, as well as the control signals. Packet arrival is also synchronized.

Once the address comparison takes place and a decision is made as to which port the packet should be switched, then all the input latches are reset by means of the control signals. The output latches store the result of the address comparison. Hence after the address comparison, even though the payload will also be processed in the same manner as the header, as all the input latches are reset, no changes would be made to the result of the address comparison. Once the packet passes through the comparator, it is switched to the appropriate port. Buffering is necessary in the processing to ensure that the packet reaches the output port without errors. This scheme therefore does not require any separate hardware for header separation, for O-E-O conversion, header rewriting and header-payload alignment. The header processing is entirely optical, meaning that no losses are induced. This also results in the consequent reduction of the processing time of the packet.

#### 4.3.2 Optical Buffering

Although packets arriving on the inputs are synchronized, there is no coordination between packet streams arriving on different inputs of the router. Since the comparison algorithm processes a single packet at a time, one or more packets may arrive during the same time-slot on different inputs destined for the same output. For this reason, buffering is required: all but one packet is delayed and subsequently transmitted to the output. The implementation of an effective buffering strategy directly in the optical domain is fundamental to router designs. Various buffering schemes that can be implemented in the all-optical router design proposed above include:

- Forward Fiber Delay Line Buffering (FDL): Here, the packet is delayed at the output port and leaves the node after the propagation delay of the FDL [13].
- Feedback FDL buffering or Re-circulating buffer: The packet is delayed and re-enters the node after the propagation delay of the FDL [14]. The advantage here is increased buffer depth, without installing extra hardware. Storage time is adjustable in this approach.
- Deflection Routing: If more than one packet arrives for a given output, all but one are deflected, that is, they are sent to the wrong output and must try to reach the correct destination node via an alternative route. This scheme is not preferred as the probability of packet being discarded is greater, and also the packet may be forwarded to the destination via a longer route [14].

- Use the wavelength dimension to reduce the amount of buffering: WDM networks provide one new additional dimension, namely wavelength, for contention resolution [15]. Wavelength conversion offers effective contention resolution, without relying on buffer memory [13]. Wavelength converters can convert wavelengths of packets that are contending (for the same wavelength) for the same output port so that they can be routed concurrently [16].

Though various implementations for optical buffering have been introduced, more research is required to develop a feasible solution for the implementation of optical buffering for an all-optical router.

## 5. Simulation

This section summarizes the different test scenarios simulated to verify the proper operation of the arterial router in a unicast Cartesian Network, with the simulation result for one of the cases described in detail. Simulations have been carried out using MATLAB 6.5 [11]. The modular functions written specifically for each optical gate are based on the mathematical model of SOA-MZI device described in [10]. On the application of pre-defined input power levels/bit values (to simulate the header of a packet), these functions are called subsequently to give an output that verifies the functionality of the circuit for the optical Arterial Router. During the simulation of the individual gates, as well as for the entire circuit of the router, the following has been maintained:

- A power level of 2dB, has been characterized as bit value of 1.
- A power level of -10 dB has been characterized as a bit value of 0.

These operating points were fixed after analyzing the parameters that were compatible to the two transfer functions (based on the mathematical model) of the SOA-MZI device depicting constructive and destructive interference.

Table 1 summarizes the five different tests performed to verify the arterial router process flow.

Although the arterial router circuit has been successfully simulated for all five cases, due to space constraints only a single test result is presented in this section<sup>1</sup>. For the purpose of the simulation, only the header portion of the packet is taken into account, wherein the first 10 bits represent the latitude and the next 10 bits represent the longitude. The following section summarizes the simulation result for the case where Destination Latitude is greater than the Local Latitude.

<sup>1</sup>See [www.dal.ca/~lhughes2/index.html](http://www.dal.ca/~lhughes2/index.html) for complete test results.

**Table 1. Arterial Router Test Scenarios**

Test Performed	Result
Destination Address = Local Address	Packet routed to local port of the router
Destination Latitude > Local Latitude	Packet routed to north port
Destination Longitude > Local Longitude	Packet forwarded to the output port
Destination Latitude < Local Latitude	Packet routed to south port
Destination Longitude < Local Longitude	Packet is discarded

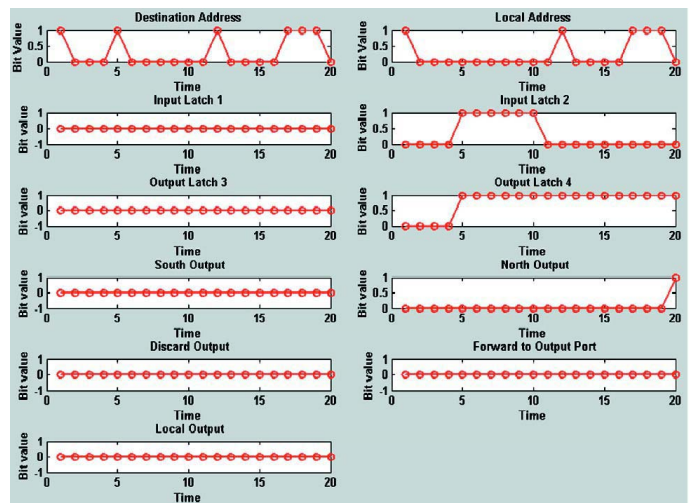
### 5.1. Destination latitude greater than local router latitude

The two address streams arrive at the input stage and are compared bit by bit. Table 2 shows the bit streams for the destination and the local latitudes.

**Table 2. Latitude Addresses**

Address Type	Bit Stream
Destination Latitude	1 0 0 0 1 0 0 0 0 0
Local Latitude	1 0 0 0 0 0 0 0 0 0

When the simulation is run with this data, an inequality is detected in the 5<sup>th</sup> bit of the latitude portion of the two addresses. As a result the output of the gate 1 (see figure 5) goes high which resets the input latch 1 and sets latch 2 (see figure 7). This in turn sets output latch 4, which indicates that the packet is to be forwarded to the north port.



**Figure 7. Simulation of Arterial Router**

As soon as the input latch of the latitude comparator is

set, it disables the input and the output latches of the longitude comparator. At the end of the latitude comparison, the Reset\_Lat signal (see figure 6) goes high and resets the input latches 1 and 2 (see figure 7), but still the output latch 4 remains set. The Longitude comparator block remains inactive during the entire address comparison. At the end of the address comparison the Latching\_Sig goes high and the packet is successfully routed to the north port, as shown by the north output in figure 7.

## 6. Conclusions and Future Work

As pervasive computing becomes more widespread, the requirement for the robust infrastructure of multiple service delivery will rise phenomenally. The speed and bandwidth requirement will shift the focus from the electronic to the optical domain for core networks. Routers for these networks will have to rely on all optical implementations. An attempt to build such a router has been described in this paper. However, more research is still needed until commercial fabrication is possible.

The next step will be to design a four port arterial router, incorporating a suitable buffering strategy. As the Cartesian topology reduces network routing time, it is an attractive alternative to network design and implementation. When deployed in an optical domain, these networks can meet the enhanced speeds and traffic requirements.

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